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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,982	10/18/2004	Juergen Pille	DE920030003US1	5981

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,982	PILLE ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 11* is/are allowed.

6)☒ Claim(s) *1-4,10 and 12* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on August 30, 1999 has been entered.

2. Claims 1-7, 9-12 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7, 9-12 have been considered but are moot in view of the new ground(s) of rejection.

4. In Remarks, claims are 1-7, 9-12, not 1-11 as reply on 01/26/2007.

5. This application contains claim 8 is withdrawn. A complete reply must include cancellation of no considered claim.

Regarding claim 8, line 1, should be replaced "Withdrawn" by –Canceled--.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-4,10,12 are rejected under 35 U.S.C. 102(e) as being anticipated by Eitrheim et al. (U.S. Patent No. 6,788,585).

Regarding claim 1, Eitrheim et al. disclose a method (ABSTRACT) for accessing memory cells within a memory array operated with a precharge mechanism, in which differential read and write access operations are performed by activating a true bitline and a complement bitline (Figures 2A-B), the method comprising:

determining whether a next memory access operation (Figure 2B, NEXT ADDRESS) occurring in a clock cycle subsequent to an access operation occurring in a current clock cycle is a read access operation or a write access operation (Column 7, lines 2-20); and

performing a precharge (column 7, lines 31-35) of the true and complement bitlines only when a read access operation follows the access operation occurring in the current clock cycle (Column 6, lines 30-34).

Regarding claim 2, Eitrheim et al. discloses wherein the memory array comprises a static random access memory (SRAM) array (column 4, line 55).

Regarding claim 3, Eitrheim et al. discloses in which a first precharge control signal is combined with a read cycle (n+1) control signal to evaluate whether a next memory access cycle comprises a read access or a write access (Figure 2B, C, Column 6, lines 32-34).

Regarding claim 4, Eitrheim et al. disclose wherein the first precharge control signal and the read cycle n+1 control signal are combined to yield a second precharge signal (Column 6, lines 29—35).

Regarding claim 10, Eitrheim et al. disclose an integrated circuit memory array adapted for low power operation (Figure 1), comprising:

a plurality of addressable memory cells (Figure 1, 16) arranged in rows and columns, the memory cells segmented into a plurality of memory blocks;

a plurality of column lines, each coupled to a corresponding column of memory cells; a plurality of row lines, each coupled to a corresponding row of memory cells (inherent in a memory device);

a precharge circuit (Figure 1, 32) coupled to the plurality of row lines, the precharge circuit provided to assert the plurality of row lines in a memory block to a high logic level following a memory access operation;

a first precharge signal controller coupled to the precharge circuit, the first precharge signal controller provided to generate a first precharge control signal (Column 5, lines 34-35;

a read cycle signal controller (Figure 1, 46, Column 6, lines 5-10) for generating a read cycle (n+ 1) signal when a next memory access operation is a read access operation; and

a multiplexer (Figure 1, 34) adapted to evaluate the first precharge control signal and the read cycle control (n+1) signal, the multiplexer asserting a second precharge

control signal when a next memory access is a read access operation for controlling the precharge circuit.

Regarding claim 12, Eitrheim et al. disclose wherein the memory array is a static random access memory (SRAM) (Column 4, lines 55).

Allowable Subject Matter

8. Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-7 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Eitrheim et al. Chung (U.S. Patent No. 6m788,585), and others, does not teach the claimed invention having wherein the read cycle (n+1) control signal is asserted according to an operating mode of the memory array, such that a write access operation occurring over a plurality of system clock cycles results in a continuous assertion of the next read cycle (n+ 1) control signal until the write access operation is complete as claim 5 disclosed, and wherein the read cycle (n+1) control signal is asserted two system clock cycles in advance of a next memory access operation during a delay between when an address of the memory array is specified and a current access operation is complete as claim 6 disclosed, and wherein the next read cycle (n+1) control signal is asserted after a delay of one clock cycle during a period of time when no memory operation is performed as claim 7 disclosed.

9. Claims 9, 11 are allowed.

Claims 9, 11 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Eitrheim et al. Chung (U.S. Patent No. 6m788,585), and others, does not teach the claimed invention having a logical AND gate adapted to evaluate the first precharge control signal and the read cycle control (n+1) signal, the logical AND gate asserting a second precharge control signal when a next memory access is a read access operation for controlling the precharge circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827